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AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/646,478
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Title: STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA

Assignee: Intel Corporation

IN THE CLAIMS

Please amend the claims as follows:

1-21. (Canceled)

22. (New) A substrate comprising:

a first conductive layer between a first dielectric layer and a second dielectric layer, the first conductive layer including a first skip via extending through the first dielectric layer and a third dielectric layer; and

a second conductive layer on the second dielectric layer, the second conductive layer including a second via extending through the second dielectric layer, the second via and the first skip via being stacked on top of one another.

- 23. (New) The substrate of claim 22 wherein the first skip via includes a longitudinal axis and the second via includes a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via.
- 24. (New) The substrate of claim 22 wherein first, second and third dielectric layers are formed on a core and the first and second conductive layers are formed on the core.
- 25. (New) The substrate of claim 22 wherein the second conductive layer is between the second dielectric layer and a fourth dielectric layer.
- 26. (New) The substrate of claim 25 further comprising a third conductive layer on the fourth dielectric layer, the third conductive layer including a third via extending through the fourth dielectric layer, the third via being stacked onto the first skip via and the second via.

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(New) The substrate of claim 26 wherein the first skip via includes a longitudinal 27. axis and the second and third vias each include a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via and the longitudinal axis of the third via.

- (New) The substrate of claim 22 wherein the first conductive layer is a patterned 28. conductive layer and the second conductive layer is a patterned conductive layer.
- (New) The substrate of claim 22 wherein the first skip via is cylindrical with a 29. diameter between 49um and 85um and the second via is cylindrical with a diameter between 49um and 85um.
- (New) The substrate of claim 22 wherein the first skip via has a length between 30. 58um and 92um and the second via has a length between 24um and 36um.

(New) A substrate comprising: 31.

a first conductive layer between a first dielectric layer and a second dielectric layer, the first conductive layer including a first skip via extending through the first dielectric layer and a third dielectric layer; and

a second conductive layer on a fourth dielectric layer, the second conductive layer including a second skip via extending through the second dielectric layer and the fourth dielectric layer, the first skip via and the second skip via being stacked on top of one another.

- (New) The substrate of claim 31 wherein the first skip via includes a longitudinal 32. axis and the second skip via includes a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via.
- (New) The substrate of claim 31 wherein first, second, third and fourth dielectric 33. layers are formed on a core and the first and second conductive layers are formed on the core.

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34. (New) The substrate of claim 31 wherein the second conductive layer is between the fourth dielectric layer and a fifth dielectric layer.

- 35. (New) The substrate of claim 34 further comprising a third conductive layer on the fifth dielectric layer, the third conductive layer including a third via extending through the fifth dielectric layer, the third via being stacked onto the first skip via and the second skip via.
- 36. (New) The substrate of claim 35 wherein the first and second skip vias each include a longitudinal axis and the third via includes a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via and the longitudinal axis of the third via.
- 37. (New) The substrate of claim 31 wherein the first conductive layer is a patterned conductive layer and the second conductive layer is a patterned conductive layer.
- 38. (New) The substrate of claim 31 wherein the first skip via is cylindrical with a diameter between 49um and 85um and the second skip via is cylindrical with a diameter between 49um and 85um.
- 39. (New) The substrate of claim 31 wherein the first skip via has a length between 58um and 92um and the second skip via has a length between 58um and 92um.